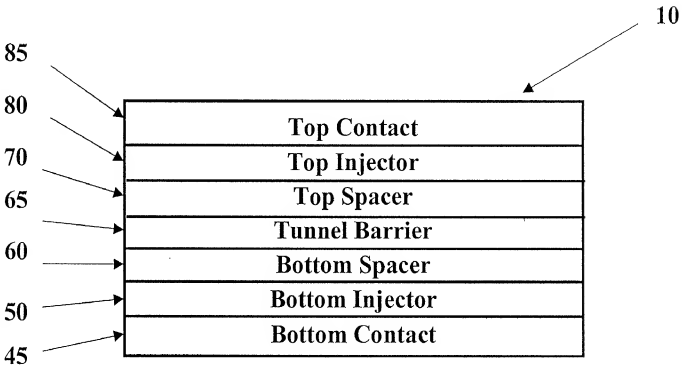


Figure 1

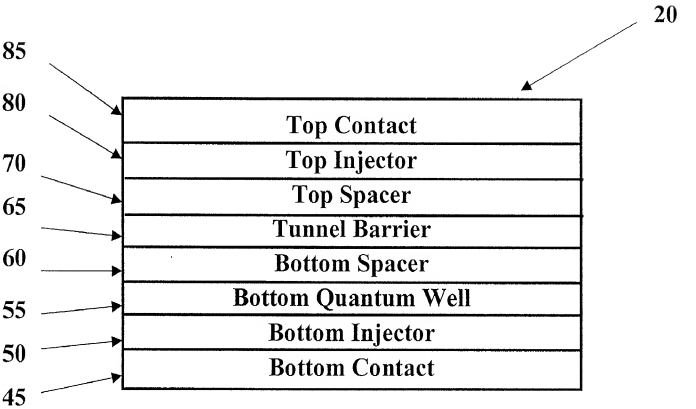


Figure 2

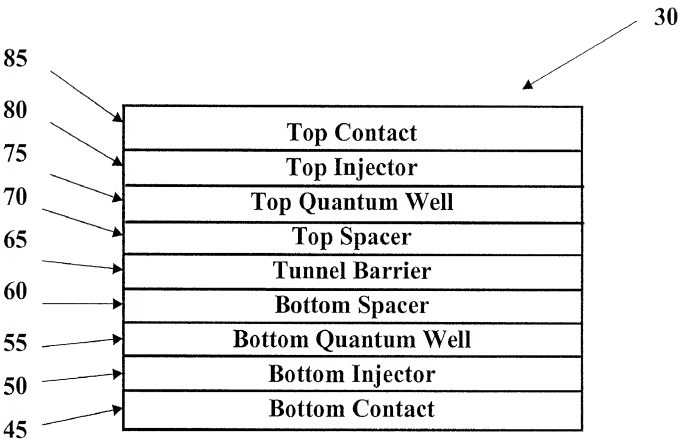


Figure 3

~50 nm n+ Si
20 nm n++ Si
4 nm undoped Si
5 nm p+Si/$Si_{0.5}Ge_{0.5}$ DG-SL 5 periods
B δ-doping plane
5 nm p^+Si/$Si_{0.5}Ge_{0.5}$ DG-SL 5 periods
100 nm p+Si
p+ Si substrate

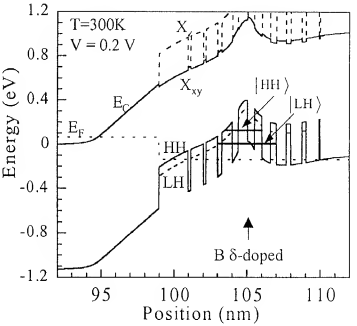


Figure 4

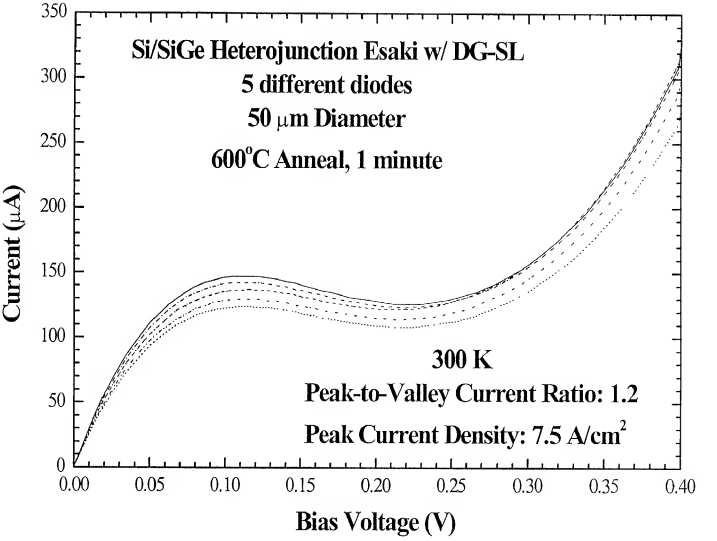
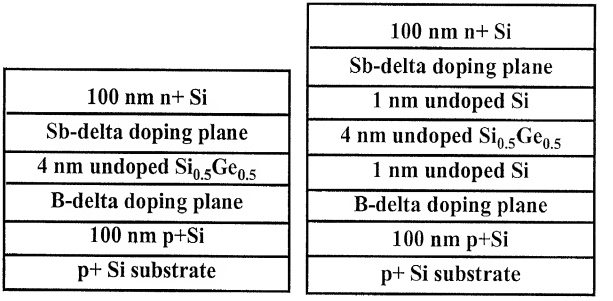


Figure 5



TD1 TD2

(a) (b)

Figure 6

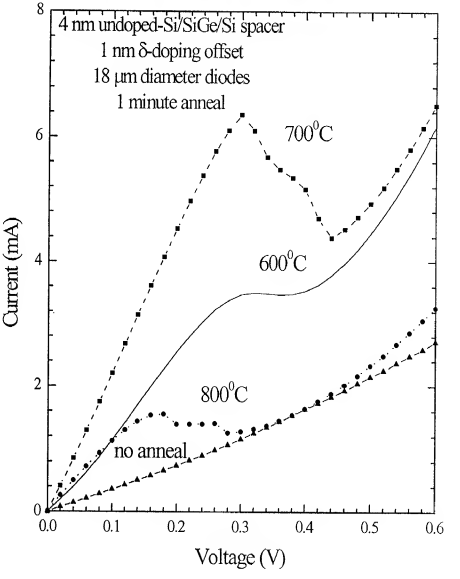
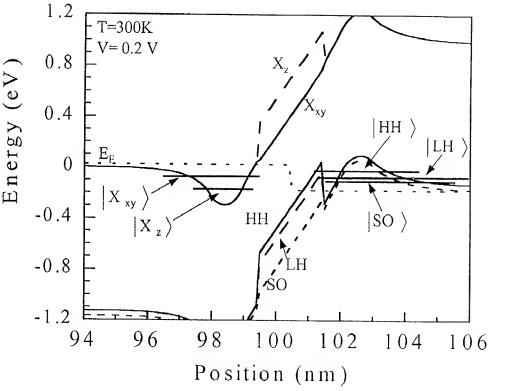


Figure 7

100 nm n+ Si
Sb δ-doping plane
1 nm undoped Si
2 nm undoped $Si_{0.5}Ge_{0.5}$
1 nm undoped Si
B δ-doping plane
100 nm p+Si
p+ Si substrate

TD3

(a)



(b)

Figure 8

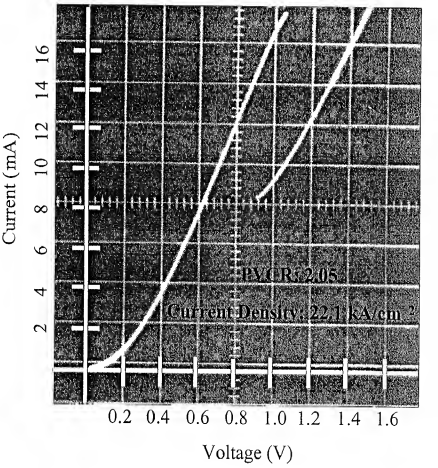
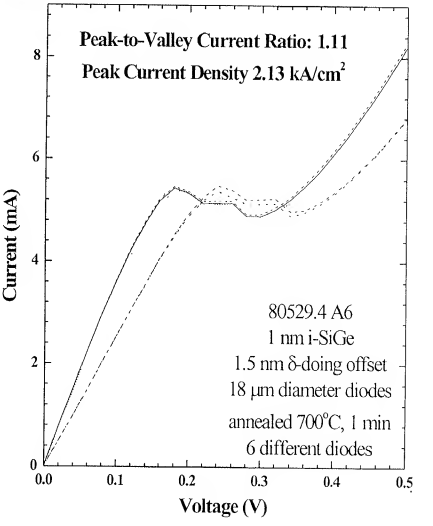


Figure 9

100 nm n+ Si
Sb δ-doping plane
1.5 nm undoped Si
1 nm undoped $Si_{0.5}Ge_{0.5}$
1.5 nm undoped Si
B δ-doping plane
100 nm p+Si
p+ Si substrate

TD4

(a)



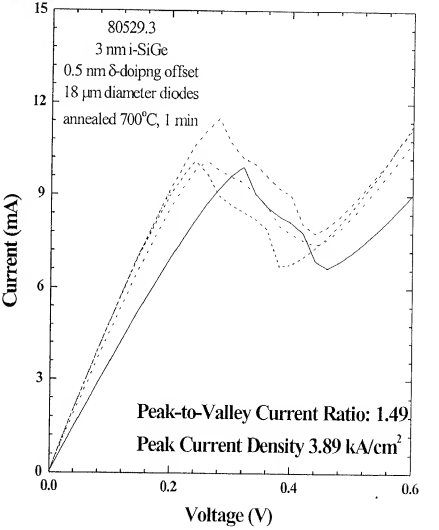
(b)

Figure 10

100 nm n+ Si
Sb δ-doping plane
0.5 nm undoped Si
3 nm undoped $Si_{0.5}Ge_{0.5}$
0.5 nm undoped Si
B δ-doping plane
100 nm p+Si
p+ Si substrate

TD5

(a)



(b)

Figure 11

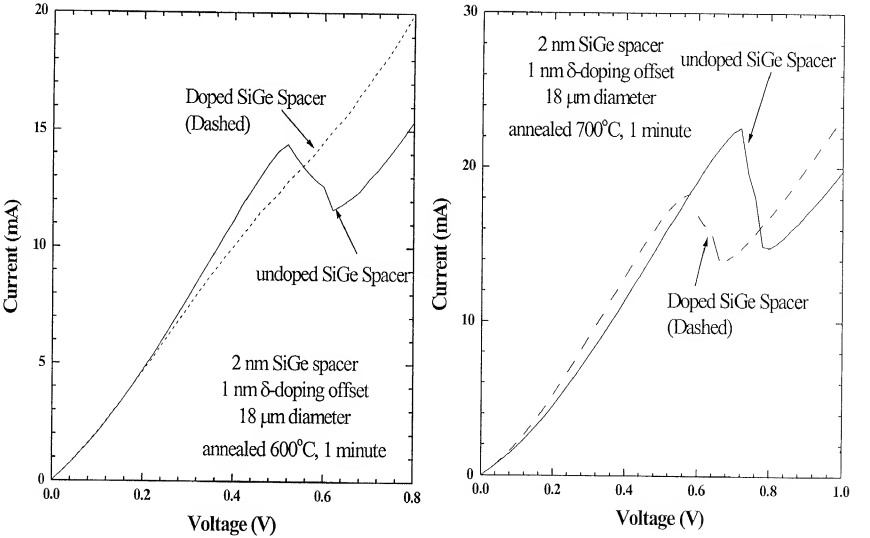
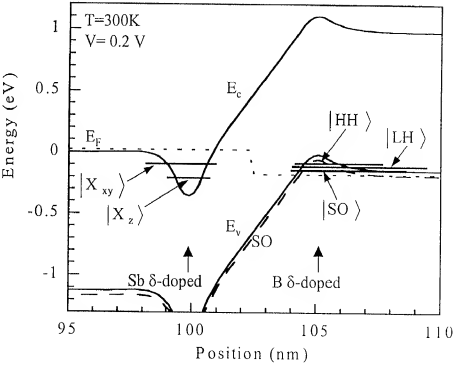


Figure 12

100 nm n+ Si
Sb δ-doping plane
4 nm undoped Si
B δ-doping plane
100 nm p+Si
p+ Si substrate

SiTD1

(a)



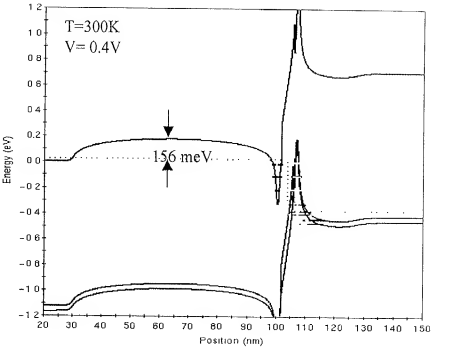
(b)

Figure 13

100 nm n-Si
Sb δ-doping plane
undoped Si Tunnel Barrier
B δ-doping plane
100 nm p-Si
p+ Si substrate

SiTD (Series II)

(a)



(b)

Figure 14

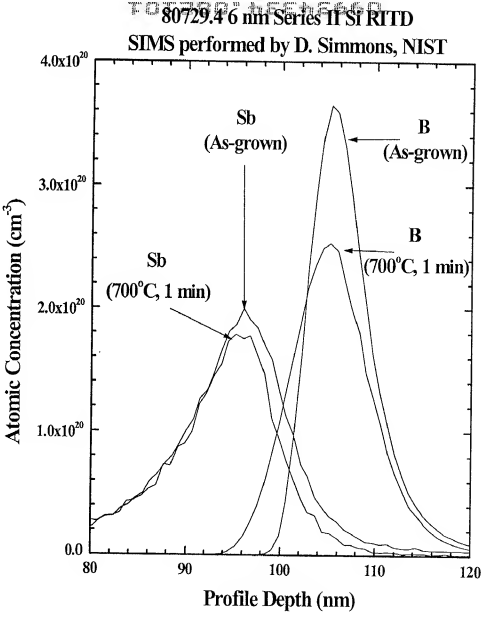

80729.4 6 nm Series II Si RITD
SIMS performed by D. Simmons, NIST
4.0x10^20
3.0x10^20
2.0x10^20
1.0x10^20
0.0
Atomic Concentration (cm^-3)
Sb
(As-grown)
B
(As-grown)
B
(700°C, 1 min)
Sb
(700°C, 1 min)
80
90
100
110
120
Profile Depth (nm)

Figure 15

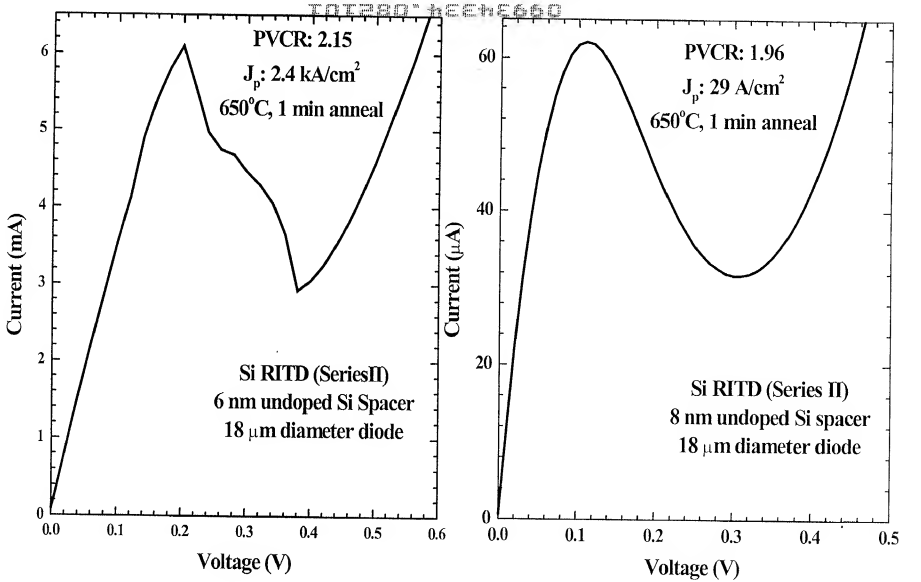

PVCR: 2.15
J_p: 2.4 kA/cm^2
650°C, 1 min anneal
Si RITD (SeriesII)
6 nm undoped Si Spacer
18 μm diameter diode
Current (mA)
Voltage (V)
(a)
PVCR: 1.96
J_p: 29 A/cm^2
650°C, 1 min anneal
Si RITD (Series II)
8 nm undoped Si spacer
18 μm diameter diode
Current (μA)
Voltage (V)
(b)

Figure 16

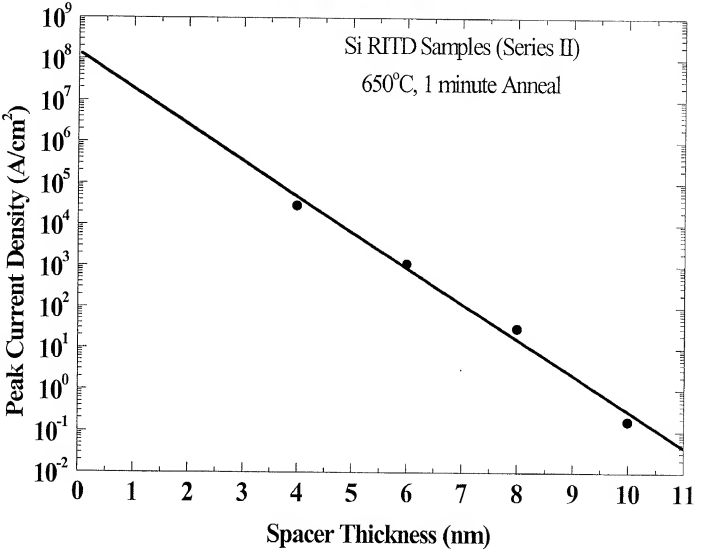
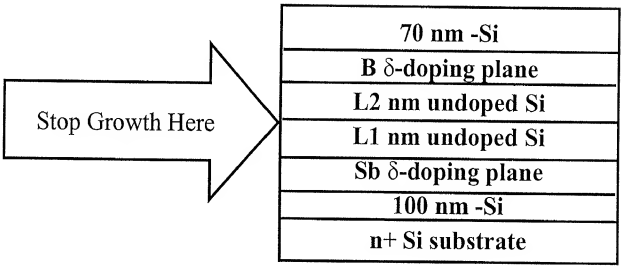
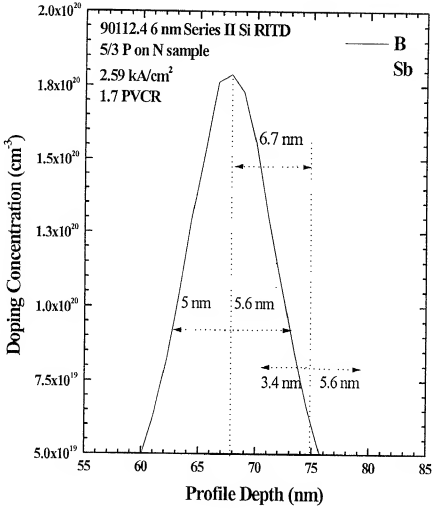


Figure 17

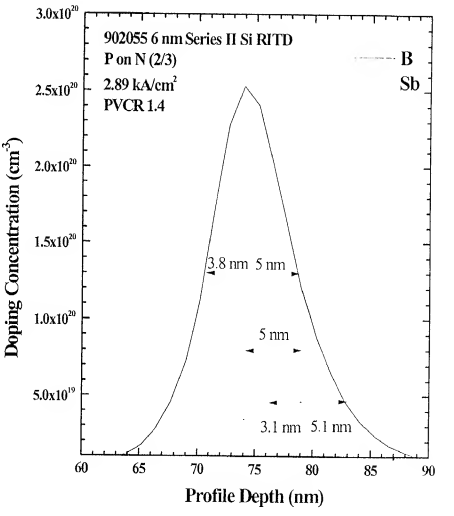


- Four combinations of **L1** and **L2** were examined:
  - **L1** = 5nm, **L2**= 9nm;
  - **L1**= 5nm, **L2**=3nm;
  - **L1**=2 nm, **L2**=3 nm;
  - **L1**=2, **L2**=6 nm.

Figure 18



(a)



(b)

Figure 19

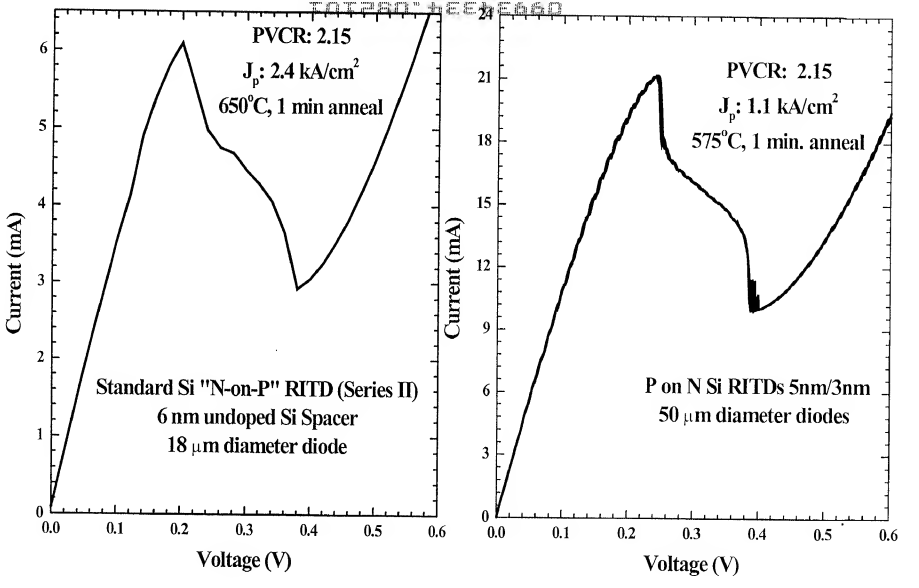

PVCR: 2.15
J_p: 2.4 kA/cm^2
650°C, 1 min anneal
Standard Si "N-on-P" RITD (Series II)
6 nm undoped Si Spacer
18 μm diameter diode
Current (mA)
Voltage (V)
(a)
PVCR: 2.15
J_p: 1.1 kA/cm^2
575°C, 1 min. anneal
P on N Si RITDs 5nm/3nm
50 μm diameter diodes
Current (mA)
Voltage (V)
(b)

Figure 20

70 nm p-Si
B δ-doping plane
6 nm undoped Si
Sb δ-doping plane
6 nm undoped Si
B δ-doping plane
100 nm p-Si
p+ Si substrate

Figure 21

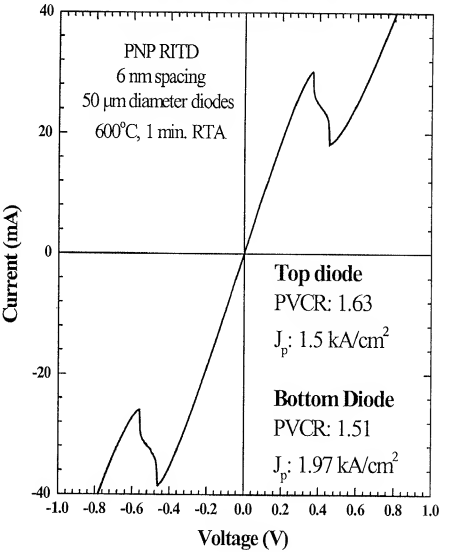


Figure 22

Sample Number	Diode Diameter (μm)	Peak Voltage (V) 700/800°C	Peak Current Density (A/cm^2) 700/800°C	PVCR 700/800°C
RITD (TD1)	18	0.35/0.12	2150/220	1.21/1.04
	50	0.55/0.25	1720/180	1.18/1.04
	75	0.68/0.36	1490/470	1.11/1.35
RITD (TD2)	18	0.34/0.16	3230/520	1.54/1.18
	50	0.87/0.38	2870/430	1.52/1.26
	75	1.21/0.52	2690/470	1.48/1.30

Table 1

1 minute anneal

		500 C	550 C	600 C	650 C	700 C
SiTD1	**Jp (A/cm2)**	1603	605	1360	872	172
4 nm i-Si	**Jv (A/cm2)**	B/w	523	982	648	149
	PVCR	Diode	1.15	1.38	1.35	1.15
SiTD2	**Jp (A/cm2)**	32000	15800	9400	1400	459
2 nm i-Si	**Jv (A/cm2)**	27000	14820	6500	1280	408
	PVCR	1.17	1.066	1.45	1.09	1.12

•NDR was observed without an anneal for SiTD1 (PVCR 1.08 , J_p=3.93 kA/cm^2)

Table 2

Table of "P on N" RITD Results
650°C, 1 min anneal

Layer	L_{before}	L_{after}	J_p	PVCR
90205.6	2 nm	6 nm	115 A/cm^2	1.2
90205.5	2 nm	3 nm	2.98 kA/cm^2	1.3
90112.4	5 nm	3 nm	2.59 kA/cm^2	1.7
90112.5	5 nm	6 nm	19 A/cm^2	1.2
90112.6	5 nm	9 nm	12.7 A/cm^2	no PVCR-inflection

- L_{before} refers to the length grown prior to the stop growth. L_{after} refers to the length after the stop growth.

Table 3